Remarks

1. Summary of Office Action

In the office action dated May 16, 2005, the Examiner rejected claims 1-12 under 35 U.S.C. § 103 as being obvious in view of Snyder (U.S. Patent No. 5,278,907) and Barron (U.S. Patent No. 6,658,112).

2. Amendments to the Claims

Applicant has amended claims 1, 4, 5, 9, 11 and 12 to emphasize that embodiments of the present application comprise a scrambling or descrambling component and an operational mode processor. The claimed operational mode processor does not scramble or descramble a received voice/data packet. Instead, the operational mode processor either vocodes or bypasses the received voice/data packet. The toggling between vocoding or bypassing is controlled via an operational mode control signal received by the operational mode processor.

Claim 1 has been amended to recite that the operational mode processor receives a signal and outputs an unscrambled signal (after vocoding or bypassing). The scrambler, also claimed in the present application, receives the unscrambled signal and it is subsequently scrambled.

Claim 4 has been amended for proper antecedent basis to amended claim 1.

Claim 5 has been amended to recite that the operational mode processor receives a descrambled signal from a descrambler and outputs a descrambled signal. The operational mode processor either vocodes or bypasses a received signal but does not scramble or descramble.

Claim 9 has been amended to recite that the operational mode processor receives an unscrambled signal, operates in accordance with the appropriate mode, and outputs an unscrambled signal. And, the operational mode processor may also receive a descrambled signal, operate in accordance with the appropriate mode, and output a descrambled signal. The operational mode

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processor receives an unscrambled or descrambled signal and outputs a respective unscrambled or descrambled signal. No scrambling or descrambling occurs within the operational mode processor.

Claim 11 has been amended to recite that the operational mode processor receives and outputs an unscrambled signal.

Claim 12 has been amended to recite that the operational mode processor receives and outputs a descrambled signal.

3. Response to the 35 U.S.C. § 103 Claim Rejections

The Examiner rejected claims 1-12 under 35 U.S.C. § 103 as being obvious in view of Snyder (U.S. Patent No. 5,278,907) and Barron (U.S. Patent No. 6,658,112). To establish a *prima facie* case of obviousness, the cited references must teach or suggest all the claim limitations. (MPEP § 2142). Applicants submit that neither Snyder nor Barron, separately or in combination, teach or suggest an operational mode processor that selects an operational mode (i.e., vocoding or voice/data bypass).

Snyder teaches a method for scrambling and de-scrambling audio and voice communications. Snyder teaches using methods such as time varying pseudo-random modification along with synchronization information in order to scramble and de-scramble a signal (Abstract). One embodiment of Snyder uses a microprocessor in combination with an inverter and a random number generator to scramble and de-scramble a signal (Col. 9, line 61 through Col. 11, line 26).

Barron, on the other hand, discloses a voice decoder that eliminates unpleasant audio due to channel errors or cryptographic synchronization loss (Abstract). Barron in itself does not disclose a method of scrambling or descrambling.

The Examiner states that Snyder fails to teach PCM signals and attempts to combine Barron to make up for this shortcoming in order to obviate the present claims. However, the combination of

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Snyder and Barron does not teach the present claims because neither reference teaches an operational mode processor. Snyder is directed to scrambling and de-scrambling audio communications. While Barron reduces offensive audio that may be associated with encryption or decryption, or other channel errors (Col. 2 lines 32-35).

In the previous office action, the Examiner maintained that that Snyder discloses "an operational mode processor" in Col. 4, lines 50-53:

> The microprocessor 26 controls operation of inverter 18 by utilizing encryption algorithm 30 to present instructions to frequency generator 28 to effectively pseudo-randomly switch the inverter 18 to present either the original audio signal or an alternate audio signal that is thus inverting the audio signal which effectively scrambles the audio signal passing through inverter 18.

The operational mode processor in Applicant's application is not used to switch between a scrambled and unscrambled signal. Instead, the operational mode processor receives an unscrambled or descrambled signal and outputs a respective unscrambled or descrambled signal in a desired operating mode. This distinction is reflected in the claims. Therefore, all of the claimed elements of Application's application are not taught by the combination of Snyder and Baron.

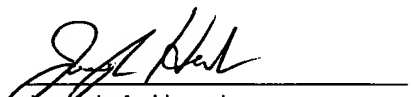
4. Conclusion

In light of these remarks, Applicants submit that claims 1-12 are in condition for allowance and respectfully request the Examiner to pass this application to issue. If the Examiner has any questions or comments, the Examiner is invited to call the undersigned agent at 312-913-3331.

Respectfully submitted,

McDONNELL BOEHNEN HULBERT & BERGHOFF LLP

Dated: July 15, 2005

By: 

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